OVERVIEW

Packet Generator is a software tool that will be running on a Host computer and generate traffic patterns. SATA packet generator is a product that generates series of High Speed Serial Packets which can be used by emulator platform to generate traffic on DUTs interfaces. Also, it can be used on Simulation platform to generate traffic on simulation environment on DUTs interface.

FEATURES

- SATA is high speed serial link.
- The serial link employed is a high-speed PHY layer that utilizes Gigabit Technology.
- It has Four 1.5 Gb/s Full Duplex SATA Ports, It generate and receive traffic on 1 to 4 SATA ports.
- Performs Sequence Control Packets – Send packets, wait-for packets, branch packets, compare packets.
- Hot-Plug Connectivity – Simulates hot-plug events by forcing the Tx lines into common-mode voltage.
- Control / Command Registers – Allows user to modify all SATA Control and Command Registers.
- Data Stream Creation – Enables easy payload generation using several data streams, including walking 1s, incrementing patterns, random patterns, and user files.
- Programmable Error Generation – Capable of sending many types of bit and protocol errors.
- Dynamic Error Injection – Allows user insertion of errors onto the SATA bus in real time.
- Event Logging – Logs several key events, such as Errors Transmitted and Data Miss-compares.
- Activity Log – Contains the information received and transmitted on the links in the past 1 ms..
- Wait States – User may set the amount of time to wait before sending the next packet. This can range from 26.67 ns to 8 hours.
- Trigger Out – Trigger out packets which allow placement of trigger points within any location in a packet stream.
- SATA uses 8b/10b encoding.

BENEFITS
• These methods can be used for verification of most complex hardware design to simple hardware design
• Easy to use solution, plug and play type solutions
• Software packet generators are very cost-effective solutions, they are cheaper compared to high license costing software products available in the market.
• Creates beautiful Emulation environment, which can mimic many simulation verification scenarios.
• Detect bug in Pre-silicon phase, which can save millions of dollars of re-spinning silicon cost.
• Post-silicon also software portion can be used for validation
• Help to build a parallel structure to simulation to find more design bugs quickly.
• The overall runtime can be reduced to as much as 10 times than long SOC simulations. This can speed up TAPE OUT of the chip.
• Score boarding and traffic analysis can be done very well in the Software solution.

GENERAL ARCHITECTURE

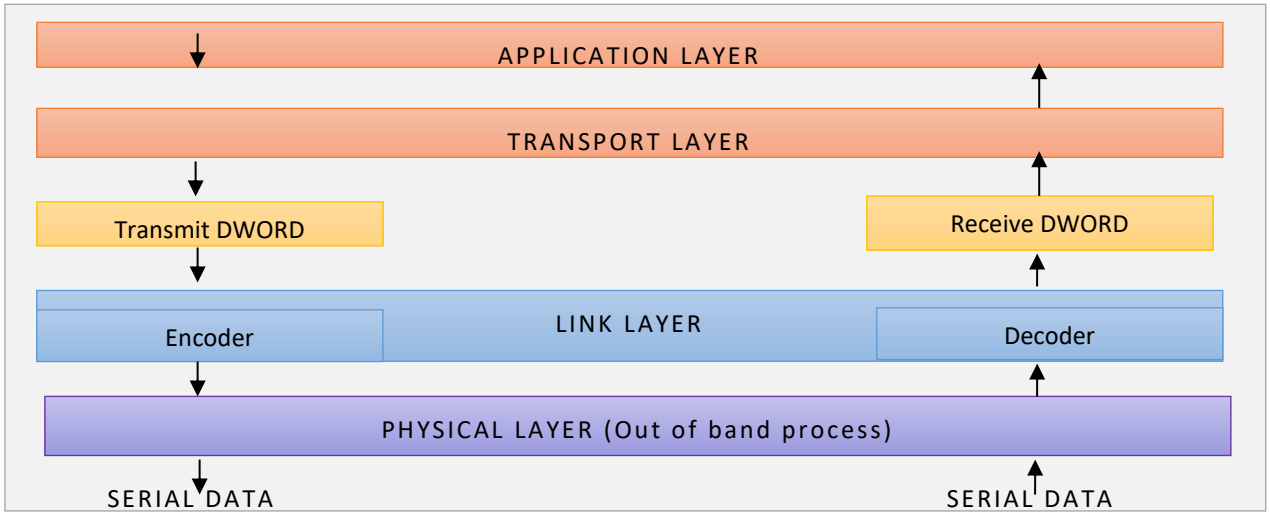

Figure 1 Layered Architecture of SATA

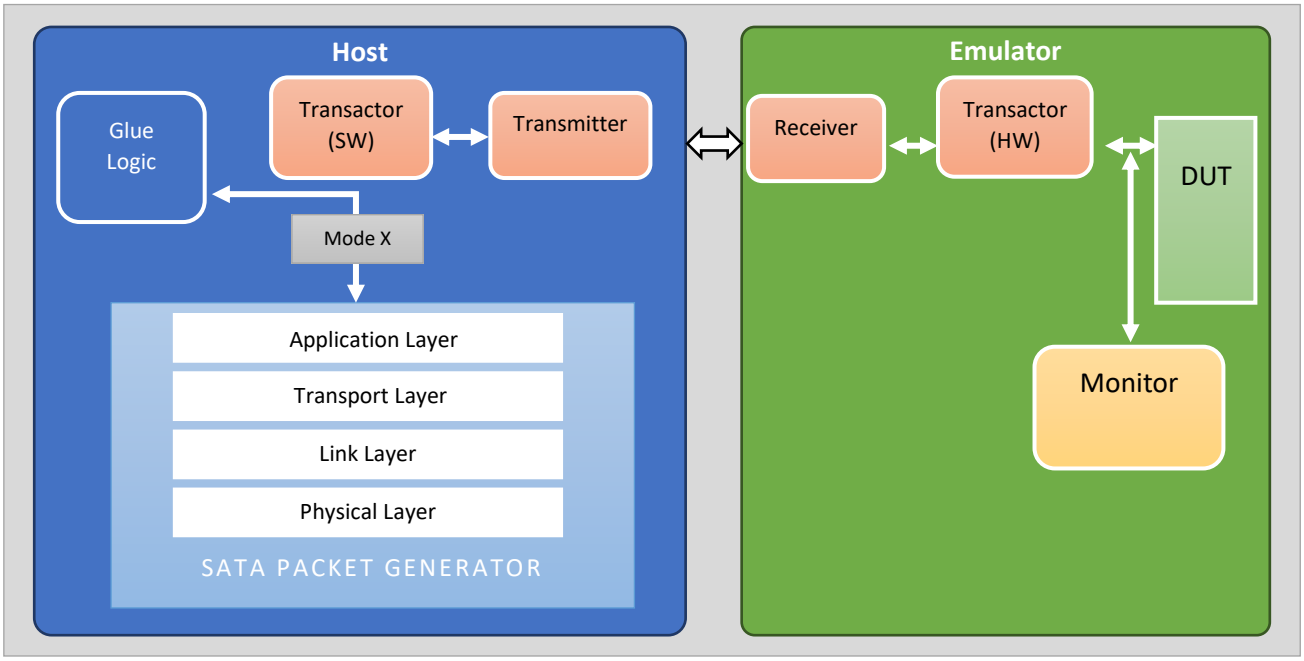

Figure 2: SATA PACKET GENERATOR in EMULATION PLATFORM

SATA FRAME FORMAT

A SATA frame consists of multiple Dwords, and always starts with SOFP, followed by a user payload called a Frame Information Structure (FIS), a CRC, and ends with EOFP. The CRC is defined to be the last non primitive Dword immediately preceding EOFP. Some number of flow control primitives (HOLDP or HOLDAP, or a CONTP stream to sustain a HOLDP or HOLDAP state) is allowed between the SOFP and EOFP primitives to throttle data flow for speed matching purposes.

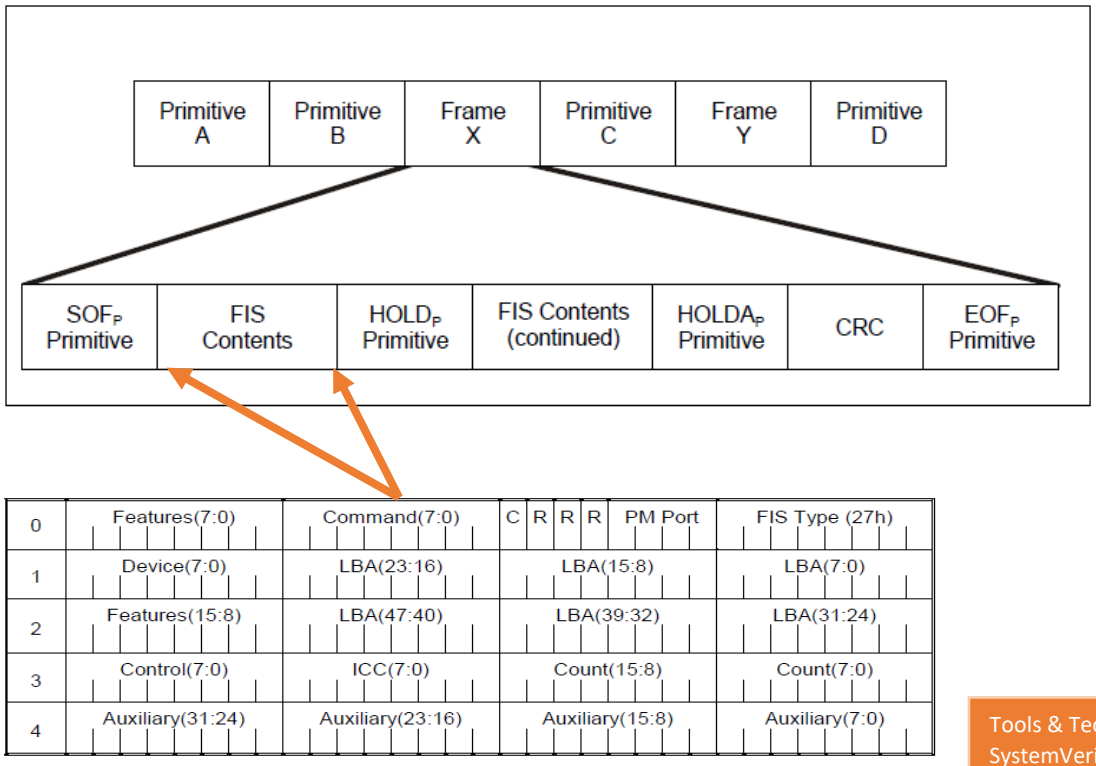

Figure 3: SATA FIS FORMAT

Tools & Technologies: Verilog, SystemVerilog, C, DPI, UVM
EDA Tools
Emulators